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Prototyping the M 68060 for concurrent verification

J Kumar - IEEE Design & Test of Computers, 1997 - [ieeexplore.ieee.org](#)

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JU Turner - ... Integrated Manufacturing, 1988., International Conference on, 1988 - ieeexplore.ieee.org

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Analysis in Solid Modeling Joshua U. Turner IBM Corporation Dept. C13/I3ldg. ...

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Tolerances in computer-aided geometric design

JU Turner, MJ Wozny - The Visual Computer, 1987 - springerlink.com

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as a processor instruction in one of these **emulation**-processors. ...[Web Search](#) - ieeexplore.ieee.org[Google Home](#) - [About Google](#) - [About Google Scholar](#)

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DS Franzblau, JC Kowalczyk - dimacs.rutgers.edu

... imaging. Excursions in Modern Mathematics (9{College) **Peter Tannenbaum**
and Robert Arnold; Prentice-Hall, 2nd Ed., 1995; \$57. This ...[View as HTML](#) - [Web Search](#) - [dimacs.rutgers.edu](#)[Google Home](#) - [About Google](#) - [About Google Scholar](#)

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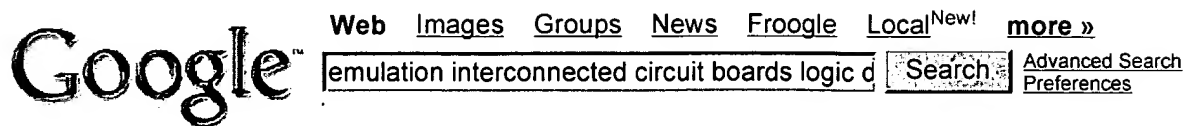
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EP259662, Method for generating a candidate list of faulty circuit elements and
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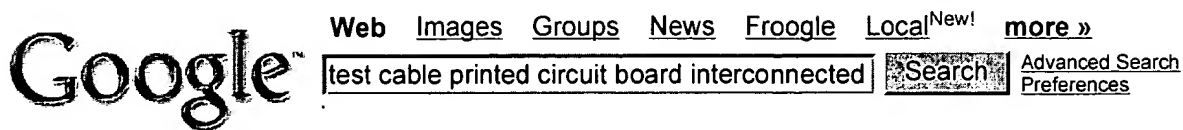
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Hardware logic emulation system capable of probing internal nodes ...

a microprocessor in-**circuit** emulator includes a **cable** which can be plugged into

a system ... and signal routing between fixed **printed circuit board** traces. ...

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Hardware logic emulation system - US Patent 5963735

an **Hardware logic emulation** system comprising: A **printed circuit board** having an

... A microprocessor in-**circuit** emulator includes A **cable** which can be ...

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Proportional to the number of events (**circuit** size* no. of cycles*Event density)

... **cable**. PSG. (pin Signal Generator). daughter **board**. chip model;ISS ...

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United States Patent Application: 0050114113

the method of claim 2, further comprising: instructing a **cable** controller to ...

a testbench is a Series of **test** vectors (ie, stimulus) that are used to ...

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Horstmann, "Marco **Test circuit** Generation," IBM TDM vol. ... A set of fixed

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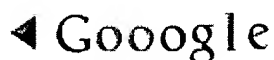
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